MINIMAL LATENCY SERIAL MEDIA INDEPENDENT INTERFACE TO MEDIA INDEPENDENT INTERFACE CONVERTER

Senthil, et al. Atty. Dkt. LSI 00-065

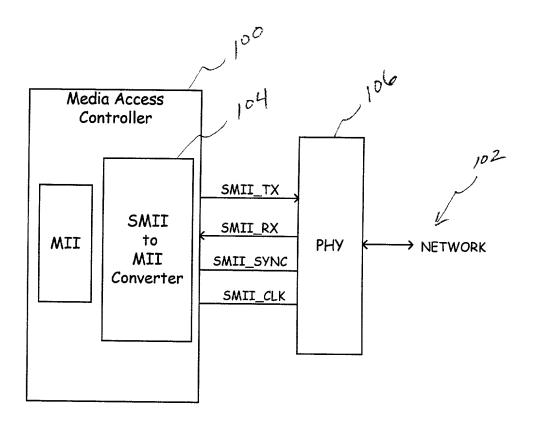


Fig. 1

MINIMAL LATENCY SERIAL MEDIA INDEPENDENT INTERFACE TO MEDIA INDEPENDENT Att. LSI 00-065 Att. LSI 00-065

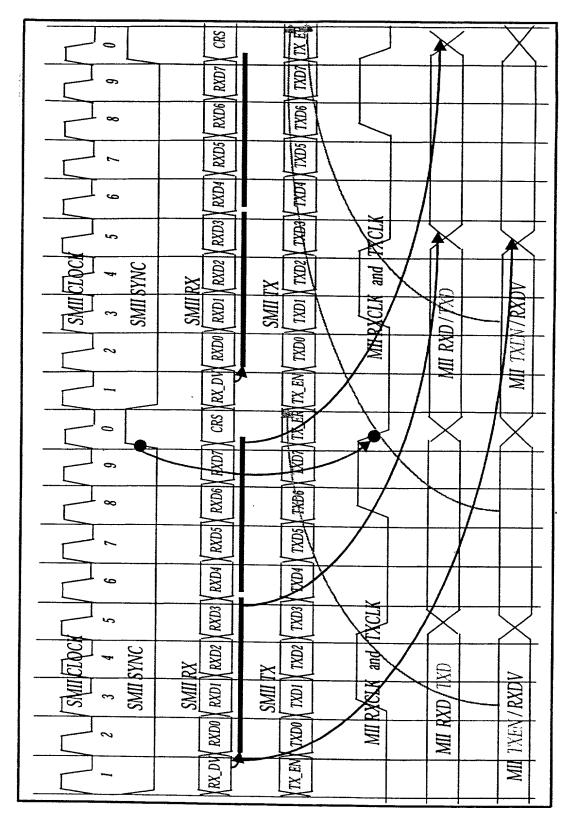


FIG. 2

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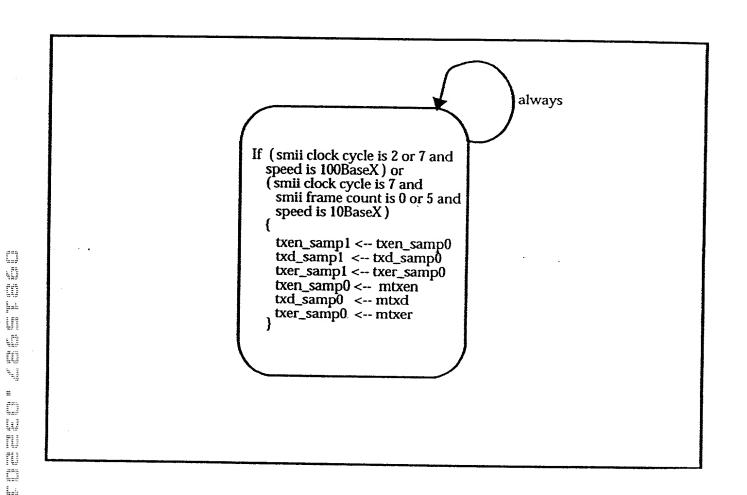


FIG. 3

MINIMAL LATENCY SERIAL MEDIA INDEPENDENT INTERFACE TO MEDIA INDEPENDENT INTERFACE CONVERTER Senthil, et al. Atty. Dkt. LSI 00-065

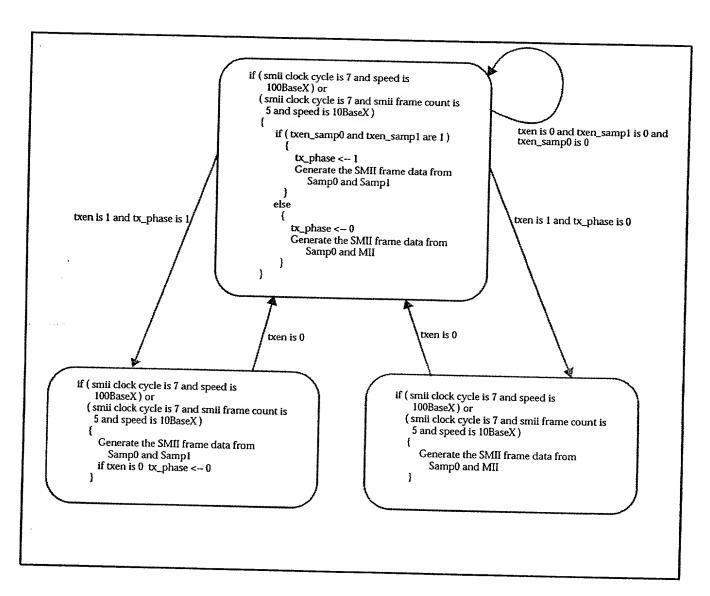


FIG. 4

MINIMAL LATENCY SERIAL MEDIA INDEPENDENT INTERFACE TO MEDIA INDEPENDENT INTERFACE CONVERTER

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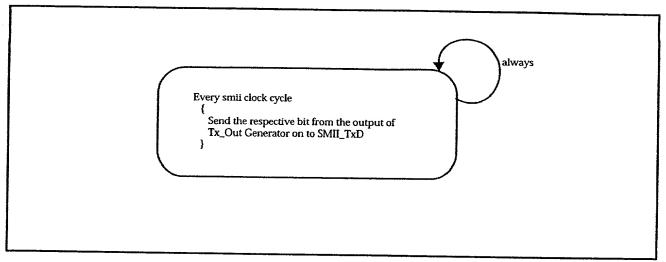


FIG. 5

```
Every smil clock cycle
{
    Register the SMII RxD input on to the respective bit of Assembled Frame
}
```

FIG. 6

MINIMAL LATENCY SERIAL MEDIA INDEPENDENT INTERFACE TO MEDIA INDEPENDENT INTERFACE CONVERTER

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```
if (smii clock cycle is 1)

{
    Generate the Rx outputs from the assembled SMII Rx data
}
    else (once in every 10th frame)
{
    Generate the Rx outputs from the 10BaseX Temp Store of SMII Rx data
}
}
```

FIG. 7